In The Claims:

1. (currently amended) A transistor comprising:

a P-substrate;

a first diffusion region and a second diffusion region formed in said P-substrate; wherein said first diffusion region and said second diffusion containing N conductivity-type ions form an N-well in said P-substrate; wherein said first diffusion region comprises an extended drain region;

a drain diffusion region containing N+ conductivity-type ions, forming a drain region in said extended drain region;

a third diffusion region containing P conductivity-type ions, comprising a P-field and divided P-fields formed in said extended drain region; ~~wherein said divided P-fields are located nearer to said drain region compared to said P-field, and wherein said P-field and said divided P-fields generate junction fields;~~

a fourth diffusion region containing P conductivity-type ions, forming an isolated P-well in said N-well formed by said second diffusion region for preventing ~~from~~ N-well's breakdown~~, wherein a left edge of the first diffusion region touches a right edge of the fourth diffusion region~~;

a source diffusion region having N+ conductivity-type ions, forming a source region in said ~~P~~N-well formed by said second diffusion region;

a channel, formed between said source region and said drain region;

a thin gate oxide layer, formed over said channel;

a polysilicon gate electrode, formed over said channel to control a current flow in said channel; ~~and~~

a contact diffusion region containing P+ conductivity-type ions, forming a contact region in said ~~P~~N-well formed by said second diffusion region ~~.~~;

a thick field oxide, formed laterally adjacent to said thin gate oxide layer;

a drain-gap, formed between said drain diffusion region and said thick field oxide to maintain a space between said drain diffusion region and said thick field oxide;

a source-gap, formed between said thick field oxide and said isolated P-well to maintain a space between said thick field oxide and said isolated P-well;

an insulation layer, covering said polysilicon gate electrode and said thick field oxide;

a drain metal contact, having a first metal electrode for contacting with said drain diffusion region; and

a source metal contact, having a second metal electrode for contacting with said source diffusion region and said contact diffusion region; wherein a left edge of the first diffusion region touches a right edge of the fourth diffusion region, said divided P-fields are located nearer to said drain region compared to said P-field, and said P-field and said divided P-fields generate junction fields.

2. (original) The transistor of claim 1, wherein said N-well formed by said second diffusion region provides a low-impedance path for said source region and restricts a transistor current flow in between said drain region and said source region.

Claim 3. (cancelled)

4. (currently amended) The transistor of claim ~~3~~ 1, further comprising:
a drain bonding pad, for connecting to said drain metal contact for a drain electrode;
a source bonding pad, for connecting to said source metal contact for a source electrode; and
a gate bonding pad, for connecting to said polysilicon gate electrode.

5. (original) The transistor of claim 1, wherein said P-field and said divided P-fields form junction-fields in said N-well to deplete a drift region.

6. (new) The transistor of claim 1, wherein the N-well has an ion-doped concentration ranging from 5E15/cm^{-3} to E16/cm^{-3}.

7. (new) The transistor of claim 1, wherein the extended drain region has an ion-doped concentration ranging from 5E15/cm^{-3} to 5E16/cm^{-3}.

8. (new) The transistor of claim 1, wherein the drain diffusion region has an ion-doped concentration ranging from 5E19/cm^{-3} to 5E20/cm^{-3}.

9. (new) The transistor of claim 1, wherein the drain region has an ion-doped concentration ranging from 5E15/cm^{-3} to 5 E16/cm^{-3}.

10. (new) The transistor of claim 1, wherein the source-gap has an ion-doped concentration ranging from 5E14/cm^{-3} to 5 E15/cm^{-3}.

11. (new) The transistor of claim 1, wherein the source diffusion region has an ion-doped concentration ranging from 5E19/cm^{-3} to 5 E20/cm^{-3}.

12. (new) The transistor of claim 1, wherein the source region has an ion-doped concentration ranging from 1E16/cm^{-3} to 1 E17/cm^{-3}.

13. (new) The transistor of claim 1, wherein the contact diffusion region has an ion-doped concentration ranging from 5E19/cm^{-3} to 5E20/cm^{-3}.